Energy – Efficient CMOS Full Adders

Branko Dokić, Miladin Sandić

Abstract - This paper gives a summary of CMOS full-adder cells topologies and their comparison from the aspect of energy efficiency. A special attention is given to Hybrid-CMOS logic style full-adders. Logic delay and power consumption are analyzed. These topologies are found in three CMOS operating modes: standard, mixed or hybrid and sub-threshold mode. These characteristics are obtained by application of the PSPICE and the parameters of 180nm technology.

Keywords - Full-adder, CMOS logic design, logic delay, low-power.

I. Introduction

Two opposed demands are often posed before a designer of a digital system: to achieve greater data process speed and lesser electrical energy consumption. A compromised solution is in one of two following strategies: lesser consumption at given frequency range or greater frequency at given maximum electric energy consumption. Therefore an energy efficient system often involves a system designed in accordance with the demands of one of two mentioned strategies. Such project is often called optimal. Optimal project includes decomposition of system architecture, a good choice of basic cell and module topology and a good choice of technology. A designer is therefore required to possess excellent knowledge of components, basic logic cell topologies and modules, and system architecture.

The strategy of minimal consumption in a given frequency range is bounded by data process speed, and also by a presented project task, technology, topology of cells for the synthesis of logic functions and by accuracy. As this includes five specifications, which can be illustrated with the fingers of the hand, this strategy is also known as “the low-power hand.” [1]

The optimization of consumption is therefore multidimensional demand which includes optimization in each design phase of a complex integrated circuit or a digital system. The greatest economization of electrical energy is realized during the opening phases of design, when the project is at the drawing board.

The first section of this paper, through several topologies of the CMOS full adder, shows how important is a good knowledge of logic possibilities of the selected technology during the design of the optimal system. Naturally, not all of the possible logic options are analyzed here, but only some representative groups.

As previously emphasized, an energy efficient system of a given technology and topology is primarily influenced by operating speed and electrical energy consumption. In CMOS technology, these two parameters depend on operating mode of CMOS logic and on the relation between supply voltage V_{DD} and the threshold voltage V_t of the MOS transistor. Afterwards we will consider the threshold voltage of nMOS and pMOS transistor as equal by absolute value, i.e. $V_{tn} = |V_{tp}| = V_t$. When $V_{DD} > 2V_t$ CMOS logic circuits are operating in the standard or conventional mode, and if $V_{DD} < V_t$ then they are in the sub-threshold CMOS operating mode. There is also the mixed or hybrid CMOS mode in the region $V_t < V_{DD} < 2V_t$ [2].

The possibilities and limitations of each CMOS operating mode are shown on the example of hybrid topology of 4-bit ripple-carry adder. The characteristics of logic delay and power consumption are obtained by the application of PSPICE program and 180 nm CMOS technology parameters.

II. Models of static CMOS adders

The basic structure of the full 1-bit adder consists of two half adder and one 2-input OR circuit. It is described by the following analytic model:

$$s_i = a_i \cdot \oplus b_i \oplus c_i$$
$$c_{i+1} = a_i \cdot b_i + (a_i \oplus b_i)\, c_i \qquad (1)$$

where a_i and b_i are both input bit operandi; c_i and c_{i+1} are input and output carry-signal respectively, and s_i is the sum. The optimal synthesis of the equation implies a minimal number of MOS transistors of the selected topology of the basic CMOS logic cells (CMOS logic).

A. Conventional logic

It is well known that the conventional logic is based on the application of trasnsistor network with one pair of nMOS and pMOS transistors on each input. It can thereby be dual or symmetrical. In the first case nMOS and pMOS networks are dual, and in the second they are symmetrical. Dual networks are standard, and symmetrical ones are applicable only in specific cases, such as binary adders.
Optimal synthesis of the full adder with the conventional logic stems from a modified system of equations of the sum

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s_i and carry c_{i+1}:[3]

$$\begin{aligned} s_i &= a_i b_i c_i + (a_i + b_i + c_i)\overline{c}_{i+1} = \overline{s}_{in} \\ c_{i+1} &= a_i b_i + (a_i + b_i)c_i = \overline{c}_{(i+1)n} \end{aligned} \quad (2)$$

The function of nMOS networks of complementary functions $\overline{s}_i$ and $\overline{c}_{i+1}$ are determined by (2), and the corresponding dual pMOS networks, obtained by replacing logic operators "·" and "+" in (2), which yields:

$$\begin{aligned} \overline{s}_{ip} &= (a_i + b_i + c_i)\cdot(\overline{c}_{i+1} + a_i b_i c_i) \\ \overline{c}_{(i+1)p} &= (a_i + b_i)\cdot(c_i + a_i b_i) \end{aligned} \quad (3)$$

Dual networks (2) and (3) have 12 inputs and as much of CMOS transistor pairs. The complements $\overline{s}_i$ and $\overline{c}_{i+1}$ signals are at the network outputs, so two more inverters would be necessary for generating s_i and c_{i+1} functions.

The output adder functions can also be implemented in symmetrical networks of CMOS transistors.[4] Since in binary algebra $a_i\, b_i\, c_i\, (a_i + b_i + c_i) = a_i\, b_i\, c_i$ or $a_i\, b_i\, (a_i + b_i) = a_i\, b_i$, the functions of pMOS networks are identical to (2), i.e. $\overline{s}_{ip} = \overline{s}_{in}$ and $\overline{c}_{(i+1)p} = \overline{c}_{(i+1)n}$.

Symmetrical or mirror adder possess the same number of MOS transistors (24) as dual adder network. The advantage of symmetrical adders is that their property of symmetry guarantees equal rise and fall time of signals s_i and $\overline{c}_{i+1}$. On the other hand, the number of serial pMOS transistors in symmetrical sum and carry networks is reduced by one, which increases their speed.

B. XOR – XNOR – MUX model

The sum and carry functions (1) of the full adder can be presented in the following form:

$$\begin{aligned} s_i &= p_i \oplus c_i \\ c_{i+1} &= \overline{p}_i a_i + p_i c_i \end{aligned} \quad (4)$$

considering that $\overline{p}_i a_i = a_i b_i$, where

$$p_i = a_i \oplus b_i \quad (5)$$

is the carry propagate signal. The adder logic scheme according to (4) consists of two XOR circuits and multiplexer 2/1 (Fig.1). The propagate signal p_i is applied to multiplexer select input.

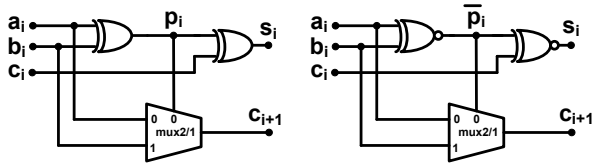

Fig. 1. XOR – MUX (a) and XNOR – MUX full adder logic schemes (b)

The XNOR logic circuits can be applied instead of XOR. This stems from the following logic model of the full adder:[5]

$$\begin{aligned} s_i &= \overline{\overline{p}_i \oplus c_i} \\ c_{i+1} &= \overline{p}_i a_i + p_i c_i \end{aligned} \quad (6)$$

This model possesses the XNOR logic circuits, instead of XOR (Fig.1b). The complement of propagate signal p_i is the multiplexer 2/1 select input.

C. Pass-transistor logic

The basic logic cell of pass-transistor logic is the transmission gate which consists of of two CMOS transistors connected in parallel. The synthesis of XOR, XNOR and MUX 2/1 functions with the transmission gates is shown in Fig. 2. [6] The sources of CMOS transistors Mn and Mp are applied to signal lines *b* and $\overline{b}$ (Fig. 2 *a* and *b*), instead to power supply lines. Weather the XOR – MUX or XNOR – MUX topology is applied, we will get the full adder with 18 transistors in total, including inverters for complements $\overline{b}$ and $\overline{p}$.

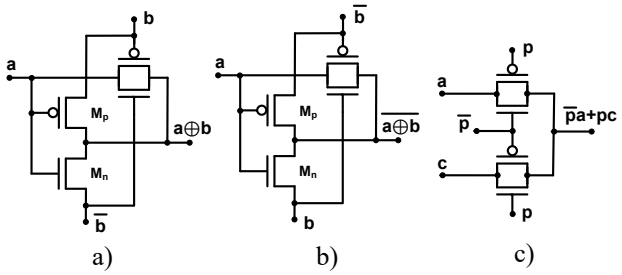

Fig. 2. Pass-transistor topologies of XOR (a), XNOR (b) and MUX 2/1 (c) circuits

D. Differential Cascade Voltage Switch Logic – DCVSL

DCVSL consists of two complementary nMOS networks with complement excitations cross-connected by two pMOS transistors [6] (Fig. 3a). Compared to the conventional CMOS logic, DCVSL has greater speed because the pMOS transistors in the transistor logic network are replaced by nMOS ones of the smaller area. Here the pMOS transistors are providing the full logic

change of the output signal from 0 to V_{DD}. The disadvantage of this logic lies in relatively great number of nMOS transistor and in the need for complement signals. The number of nMOS transistors can be decreased if there is a possibility of two networks sharing a transistor, like in XOR/XNOR circuits (Fig. 3a). Additional decrease in transistors is obtained by applying the source to signal lines, instead to the ground, as suggested in [5] (Fig. 3b).

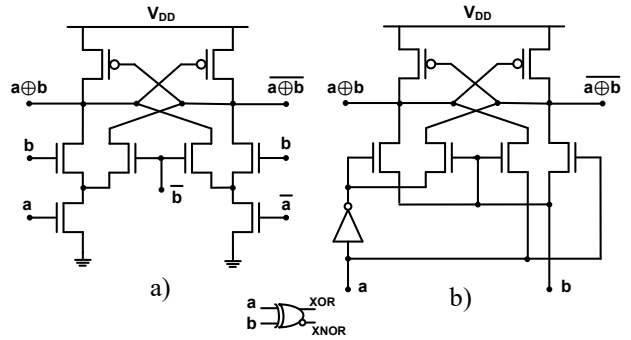

Fig. 3. DCVSL XOR/XNOR circuits

III. 4-BIT RIPPLE-CARRY ADDER

This chapter analyses the consumption and delay characteristics of the 4-bit ripple-carry adder. As already known, it consists of four 1-bit adders interconnected trough input and output carry signals. The topology of hybrid full adder [5] (Fig. 4) based on XOR-XNOR-MUX models is applied in this paper. The XOR-XNOR DCVSL. circuit for generating p_i and $\overline{p}_i$ signals is used. The module for generating the sum is a transmission-function implementation of the XNOR logic. The carry signal is generated by the hybrid-CMOS MUX 2/1, which is consisted of symmetrical logic circuits with inputs a_i and b_i and a transmission gate with input $\overline{c}_i$. The static inverters on outputs s and c_o provide good driving capabilities.

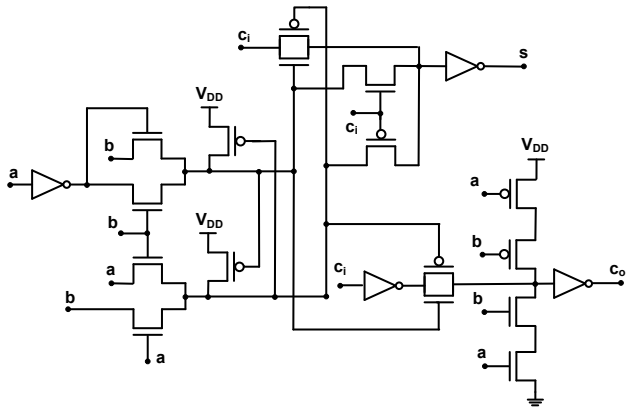

Fig. 4. Hybrid full adder

A. SPICE simulation

The characteristics of logic delay and electrical energy consumption of a 4-bit parallel repple carry adder with hybrid logic of 1-bit adder are obtained with SPICE analysis by the implementation of program package ORCAD 16.3 (Cadence Design Systems) and with 180nm CMOS technology. The threshold voltages of all MOS transistors are $Vt = Vtn = |Vtp|$ = 370mV, and channel width of nMOS and pMOS transistors, respectively, Wn = 0.3µm and Wp = 0.8 µm. The analysis includes all three CMOS operating modes while some other authors only provide the characteristics of the conventional mode.

As previously stated, there are three CMOS operating modes: sub-threshold ($V_{DD} < V_t$), mixed or hybrid ($V_t < V_{DD} < 2V_t$) and conventional or standard ($V_{DD} > 2V_t$). For that reason we have simulated the characteristics in the voltage range $200mV \leq V_{DD} \leq 2V$. Hence, within the range of $200mV \leq V_{DD} < 370mV$ is the sub-threshold mode, within $370mV < V_{DD} < 740mV$ is the mixed mode, and within $740mV < V_{DD} \leq 2V$ is the standard CMOS mode.

Fig. 5 shows the dependency of logic delay on supply voltage and on load capacitance C_L, as a parameter applied on the output carry node. In the sub-threshold region logic delay is exponentially decreasing function of the supply voltage. For C_L = 1f F, $td \approx$ 20µs at V_{DD} = 200mV, and $t_d \approx$ 0.9µs at V_{DD} = 350mV. In the mixed and standard CMOS mode $td \sim 1/V_{DD}$. For C_L = 1fF, in the mixed mode $t_d \approx$ 0.3µs at V_{DD} = 400mV, and $td \approx$ 5.5ns at V_{DD} = 700mV, while in the standard mode $t_d \approx$ 3ns at V_{DD} = 800mV and $t_d \approx$ 0.6ns at V_{DD} = 2V.

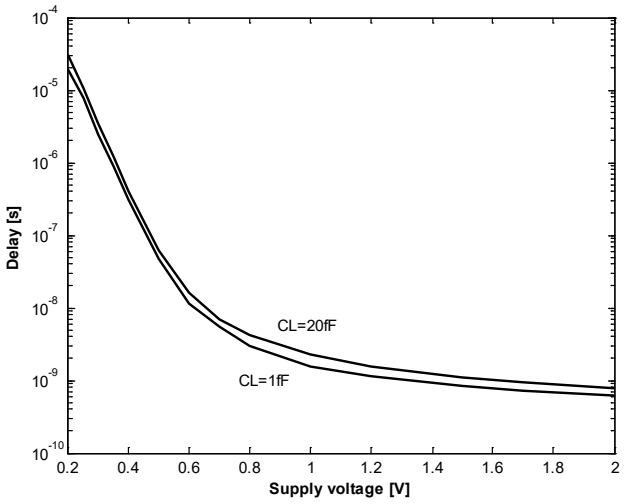

Fig. 5. Logic delay versus supply voltage

The electrical energy consumption as a function of supply voltage is shown in Fig.6. The total consumption in the sub-threshold mode is changing from 40pW to about 0.4nW, in the mixed mode from about 0.8nW to approximately 7.5nW, and in the conventional mode from about 10nW to approximately 600nW.

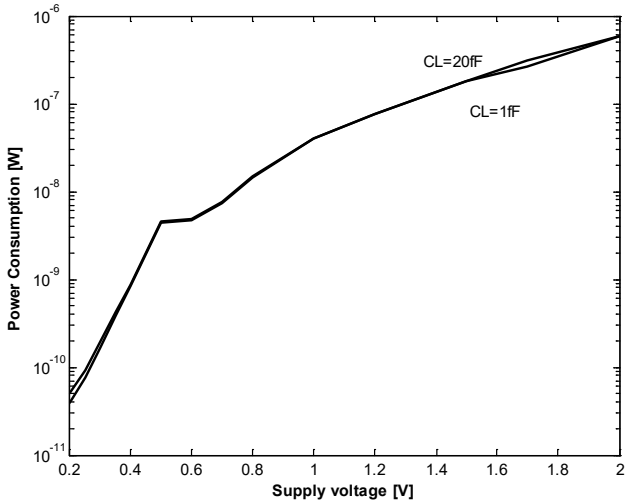

Fig. 6. Power consumption versus V_{DD}

Fig. 7. shows the consumption dependency on the logic delay. The scale of both axis is logarithmic. As expected, the smaller logic delay is, the consumption is bigger and vice versa.

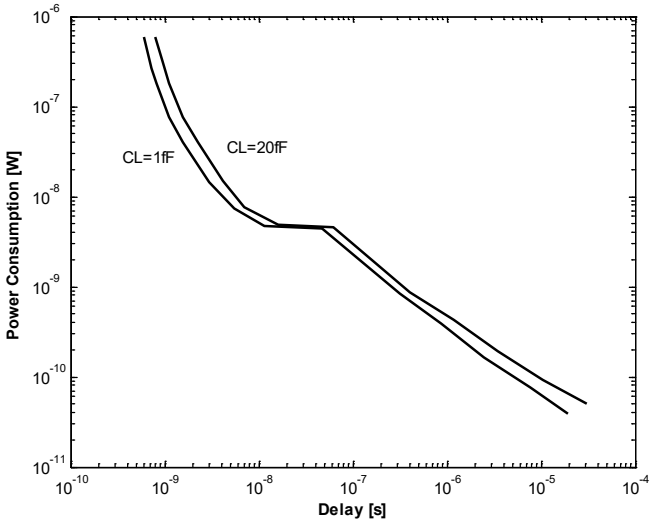

Fig. 7. Power consumption versus logic delay

The best measure of energy efficiency is the power-delay product–PDP (Fig.8). As shown in Fig. 8, the minimum PDP value is in the mixed CMOS mode.

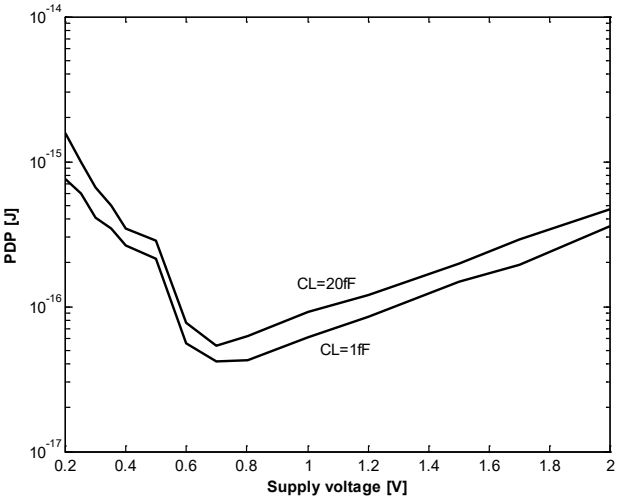

Fig. 8. Power delay product versus V_{DD}

III. CONCLUSION

The adders with pass transistor and DCVSL logic show better characteristics of consumption and delay times than those with conventional logic. The best results are obtained by implementing the hybrid logic. The electrical energy consumption of the hybrid 4-bit parallel ripple-carry adder is ranging from several dozen do several hundred *pW* in the sub-threshold mode, and around ten *nW* to several hundred *nW* in the standard CMOS mode. The logic delay in the sub-threshold mode is in the *μs* range, and within *ns* in the conventional mode. The minimal value of power-delay product in the function of supply voltage is in the mixed mode.

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