The Power Quality Estimation by Integrated Power Meter DSP Block

Borisav Jovanović, Predrag Petković, Milunka Damnjanović

Abstract - The paper considers the main features of the digital signal processing block which is embedded in a three-phase integrated power meter IC. The DSP block adds new features to modern power metering units including power quality measurement. The operations that DSP performs, are described thoroughly in the paper.

Keywords - Digital signal processing.

I. Introduction

Recent integrated circuit (IC) fabrication technologies enabled design of complex systems on the same chip area, greater clock frequencies and less dynamic component of power consumption. A representative of such complex electronic system is an integrated power meter, which digital signal processing (DSP) block is proposed in the paper. The DSP is dedicated for utilization in power metering systems. The paper explains the most significant DSP's features, which enables its integration in modern smart power meters.

Present power metering units rarely provide power quality information. Although there are several commercially available ICs dedicated to power metering applications, none of these solutions provides all necessary power quality information, important in the electrical grid systems with nonlinear loads. Present power metering units are not able to detect and quantify the distortion level at consumer site. Instead, expensive methods and devices are used, usually at higher levels of electrical energy distribution.

Previous versions of designed DSP block [1] were dedicated principally to metering of power consumption. The chip has ability to calculate root mean square values of voltage and current, active, reactive, apparent power and energy. In addition to results related to power consumption and energy, novel DSP provides several power quality measures. To quantify power quality, DSP calculates distortion power (D) and total harmonic distortion (THD) Moreover, the presence of voltage signal sags can be detected. Incorporated in power metering unit, the power signal quality is determined at sites where consumers access the electrical grid.

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II. The digital signal processing (DSP) block

A. The DSP's main features

DSP is a part of Integrated power meter chip which contains also Sigma-delta AD converters [2], digital filters and an 8051 microcontroller. At inputs, the DSP gets digital samples from the other blocks - the Sinc and FIR digital filters (Fig.1). The input signals consist of current I, voltage V and phase shifted voltage V_P for all three power grid phases. Besides them, DSP gets the digital samples of instantaneous neutral line current value and chip temperature gets. The sampling frequency of these signals is 4000 samples per second, and signal resolution is 18 bits. The DSP operates at clock frequency equal to 8.192 MHz.

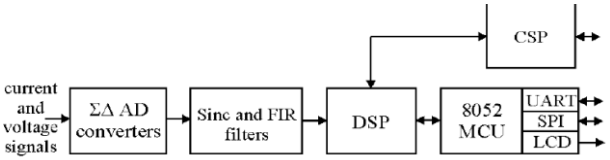

Fig. 1. The DSP block as a part of Integrated power meter

The DSP periodically, once in one second time interval, calculates following parameters:

- root mean square values of current I_{RMS} and voltage V_{RMS} for all three phases,
- root mean square value of neutral line current I_{NULL},
- the chip temperature T,
- average active P_{AV}, reactive Q_{AV}, distortion D and apparent S power in all three phases,
- power factor $Cos(\varphi)$,
- the voltage signal frequency f_{LINE},
- the values of 1., 3., 5. and 7. harmonic of current signal in all three phases,
- the current signal THD values,
- values of first harmonic of voltage signal in all three phases,
- voltage signal THD factor.

The input dynamic range for current is from 10mA to 100A and for voltage is up to 300V. The results are obtained for all three electrical grid phases.

B. The main architecture of DSP

The DSP architecture can be divided into data path and

control unit. The data path is comprised of five smaller sub blocks, denoted with Block 1 to Block 5, and additional serial communication block.

Block 1 performs arithmetically intensive calculations, including the accumulation of instantaneous samples of I^2, V^2, P and Q. The sums are needed for calculation of I_{RMS}, V_{RMS}, P_{AV} and Q_{AV}. The Block 1 measures the active, reactive and apparent energy. The Block 1 operations will be further described in detail.

Block 2 is used for calculation of: root mean square values V_{RMS} and I_{RMS}, the power factor $Cos(\varphi)$, the active P_{AV}, reactive Q_{AV}, distortion D and apparent power S, chip temperature T, the voltage signal frequency f_{LINE}, the first harmonic for voltage signal, the 1., 3., 5. and 7. harmonic for of current signal.

Block 3 calculates intermediate results that are needed for calculation of current and voltage harmonics and later, corresponding THD factors. Block 2 uses these intermediate results during its calculation process.

Block 4 is 512x24 bits RAM memory block. The RAM is used for storing the calibration data, final and intermediate results that DSP calculates.

Block 5 is a control unit. It is implemented as finite state machine, periodically performing the state sequence lasting 2048 clock cycles. The state sequence is repeated 4000 times during one-second time interval. The state sequence can be divided into four equal intervals consisting of 512 clock cycles denoted as R, S, T and E.

The DSP block results are available to external microprocessor systems (Baseband processor) through serial communication interface. The Baseband processor is able to loads the DSP's calibration registers or to read the measurement results. This feature adds flexibility to the proposed system, which causes that the DSP can be easily embedded in many power grid-metering devices.

C. DSP's control unit operation

The control unit is comprised of four smaller control units; three of them are physically implemented in blocks 1, 2 and 3. The units control the following operations:

- data transfer inside the data path blocks,
- data path transfer at block's interface,
- arithmetical calculations.

The Fig. 2 presents main control unit intervals. During intervals R, S and T, Block 1 calculates instantaneous values of I^2 voltage V^2, active P and reactive power Q. These operations are identical for different phases, except the data is stored at different locations of RAM memory. During R, S and T, Block 3 calculates intermediate results, which are further used for current and voltage signal harmonics and THD factors.

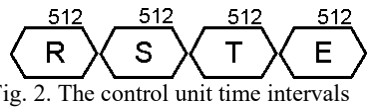

Fig. 2. The control unit time intervals

During interval E, Block 2 calculates final results - V_{RMS}, I_{RMS}, $Cos(\varphi)$, P_{AV}, Q_{AV}, S, D, chip temperature, frequency, harmonics and THD values. After chip is reset, E subsequence is also used for DSP's initialization (loading the DC offset and gain calibration registers for current and voltage signals).

D. The arithmetical operations performed by Block 1

Control unit 1 performs identical sequences in phases R, S and T. The operations are executed 4000 times per second. At the beginning of sequence, DC offset is suppressed in current, voltage and phase-shifted voltage signals. The DC offset can be rejected by High pass filter (HPF) or after DC offset is subtracted from instantaneous current and voltage values (Fig. 3). An Infinite Impulse Filter (IIR) which cut-off frequency is set to 5Hz implements the High pass filter. The transfer function of High pass filter is:

$$H_{HPF}(z) = (1-2^{-10})\frac{(1-z^{-1})}{1-z^{-1}(1-2^{-9})} \tag{1}$$

The Eq. (1) is transformed into Eq. (2), where filter register are expressed in form of RAM memory registers:

$$Ifilt = Ifilt(1-\frac{1}{2^9}) + (2^{10}-1)(I1-I3) \tag{2}$$

$$I2 = Ifilt/1024 \tag{3}$$

In Eq. (2) and (3) I_1 and I_3 are two consecutive current samples, I_{filt} is the 48-bit HPF filter register, which content is equal to current AC component, multiplied with 1024. The signal I_2 in Eq. (3) is AC component of current signal. Arithmetical units within Block 1 perform all arithmetical operation (addition, subtraction and shifting). The identical sequence of operation is executed for voltage DC offset discrimination (Fig.3).

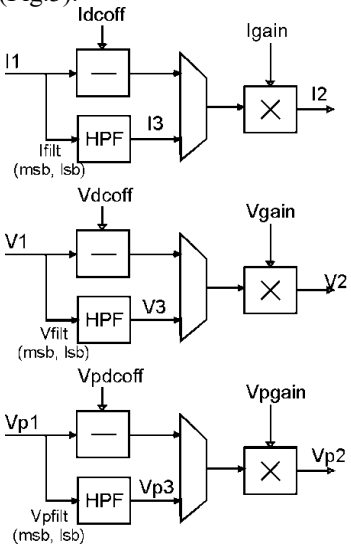

Fig. 3. The operations for DC offset eliminations

The AC component of current signal I_2 is first squared. Then, the squared result is passed through Low-pass filter.

The result is accumulated in the register AccI2.

The LPF is implemented as an IIR filter and has main goal to reduce I_{RMS} calculation error. Namely, LPF decreases AC component of square of instantaneous current signal. The chosen cut-off frequency is 10Hz. The filter's transfer function is:

$$H_{LPF}(z) = \frac{2^{-6}}{1 - z^{-1}(1 - 2^{-6})} \quad (4)$$

The transfer function can be rearranged to:

$$I2filt = I2filt(1 - \frac{1}{2^6}) + I2xI2 \quad (5)$$

$$(I2xI2)_{DC} = Ifilt / 64 \quad (6)$$

where I_2 is an AC component of instantaneous current and *I2xI2* is its squared value. The *I2filt* is 48-bit IIR filter register. The DC component is obtained after dividing the number I2filt by constant 64. At the end, the result is added to AccI2 (Fig. 4). Similar operations are performed by Block 1 for voltage signal processing. The following registers are used: 24-bit V2, 48-bit HPF register V2filt and 48-bit register AccV2. The active and reactive instantaneous power are processed similarly (presented in Fig. 4).

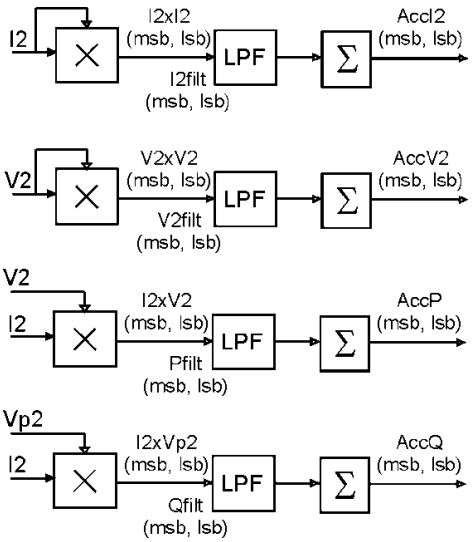

Fig. 4. The operations for multiplication, filtering and accumulation of AC components of current, voltage and phase shifted voltage signals.

E. The arithmetical operations performed by Block 2

During E subsequence (Fig. 2) operators in Block 2 calculate final results - V_{RMS}, I_{RMS}, *Cos*(φ), P_{AV}, Q_{AV}, *S* and *D*. Based on AccI2, I_{RMS} is derived as the result of following operations. First, AccI2 is divided by number 4000 - the number of accumulation operations in I_{RMS} calculation period. Then, the AC offset (I2off in Fig.5) is subtracted (shown in Fig.6). I_{RMS} is obtained after square root operation is performed.

The same hardware is used for V_{RMS} calculation. At start of operation, the AccV2 is used. For offset correction the register V2off is used. The final result is stored in register V_{RMS}.

The similar method is used for calculation of P_{AV} and Q_{AV}. The difference is that there is not square root operation (Fig.5).

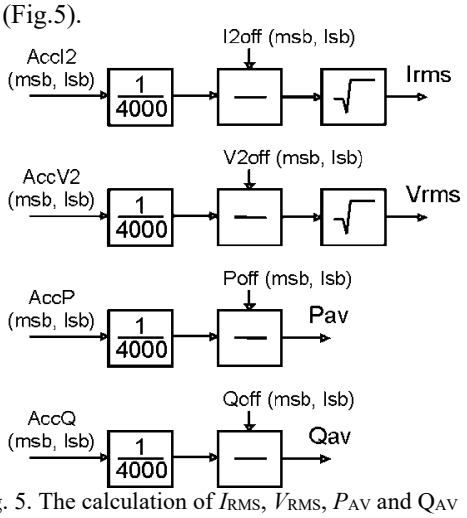

Fig. 5. The calculation of I_{RMS}, V_{RMS}, P_{AV} and Q_{AV}

The apparent power S is obtained when I_{RMS} and V_{RMS} are multiplied. After that, average active power P_{AV}, reactive power Q_{AV} and apparent power S are used for calculation of distortion power D [3], [4]. The operation sequence is given in the Fig. 6.

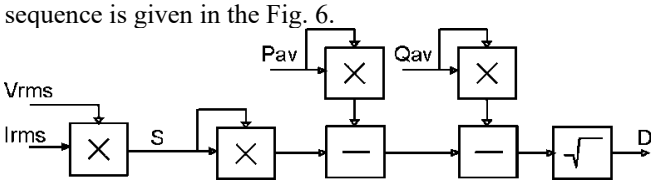

Fig. 6. The calculation of apparent power S and distortion D

F. The active, reactive and apparent energy measurement

New results for P_{AV}, Q_{AV} and S are obtained every second and they are used for measurement of active, reactive and apparent energy. The DSP block has six pins for the energy results. The pins are named with Pulse 1 to Pulse 6. The pulses are programmed in DSP's control registers:

- if pin produces the pulses for some particular phase or all three phases,
- if pin produces pulses for active, reactive or apparent power
- if positive or negative energy is measured
- the pulse width can be changed in range from 10 to 40 ms

To generate pulses for measured active energy, P_{AV} is accumulated in 48-bit register AccEa (the part of RAM memory). After the addition operation is performed, the AccEa is compared to referent energy value (stored in register Energy_P). If AccEa is greater than Energu_P, a

pulse is on output pin is generated. If active power value P_{AV} is negative (in case when electricity generators are measured), when the negative sum AccEa is obtained, a pulse for negative energy is generated and Energy_P is added to AccEa. The hexadecimal value Energy_P=0x1E000000 gives the proportion of 1000 pulses for energy of 1kWhr. This proportion can be changed in the range from 100 to 100000 pulses per 1kWhr.

The similar operations are executed for reactive energy measurement. The registers Q_{AV}, Energy_Q and AccEq are used. The Energy_ Q defines the number of pulses per 1kVaR.

G. Power quality - the harmonics and THD calculation

The Goerzel algorithm [5] has been implemented for calculation of 1., 3., 5. and 7. harmonics for the current signal. Additionally, the DSP provides that harmonic order can be changed. The order is specified by a DSP control register.

The circuit gets at inputs current and voltage samples, at 4000Hz sampling frequency. The Goertzel algorithm consists of two parts: the iterative and final part. The iterative part is executed 4000 times per second. In final algorithm step, the real and imaginary parts of complex spectral component are found. The iterative part of algorithm is executed by Block 3, while the final part is done within Block 2.

The method for obtaining the k. harmonic is described as follows. In the method, as auxiliary registers, the 48- bit Q_0, Q_1 and Q_2 are used. At the beginning of iterative operation, Q_0, Q_1 and Q_2 are reset. Next, in every iteration step, for each input sample, new values of Q_0, Q_1 and Q_2 are derived [5] according to:

$$\begin{aligned} Q_0 &= 2 \cdot Q_1 \cdot \cos(2\pi \cdot \frac{50 \cdot k}{4000}) - Q_2 + X_{IN}; \\ Q_2 &= Q_1; \\ Q_1 &= Q_0 \end{aligned} \tag{7}$$

At the end of iterative algorithm part, the real and imaginary parts of a complex number are:

$$\begin{aligned} real &= \frac{1}{2000}\left(Q_1 - Q_2 \cdot \cos(2\pi \cdot \frac{50 \cdot k}{4000})\right) \\ imag &= \frac{Q_2 \cdot}{2000} \cdot \sin(2\pi \cdot \frac{50 \cdot k}{4000}) \end{aligned} \tag{8}$$

The k. harmonic is found as:

$$y^k = \sqrt{real^2 + imag^2} \tag{9}$$

The harmonics are stored in 24-bit registers. The circuit calculates the THD factor [5]:

$$THD = \frac{1}{I_{1,RMS}} \sqrt{I_{RMS}{}^2 - I_{1,RMS}{}^2} \tag{10}$$

H. Implementation results

The DSP block is successfully verified after extensive simulations are performed. The parts of a DSP circuit, which calculates the electrical power system parameters, are particularly verified. The circuit has been implemented in technology AMI 180nm and occupies 0.5mm^2 area.

III. Conclusion

Many different power metering functions are implemented in the same chip. DSP achieves high performances at the levels as those obtained with commercial DSP microprocessors and consumes less power consumption. Since it calculates harmonics, THD and distortion power, the DSP can be easily embedded in devices dedicated to power quality measurement, especially when nonlinear loads are present in the grid.

Acknowledgement

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References

[1] Jovanović, B., Damnjanović, M., Petković, P., "*Digital Signal Processing for an Integrated Power Meter*", Proceedings of 49. Internationales Wissenschaftliches Kolloquium, Technische Universitat Ilmenau, Ilmenau, ISBN 3-8322-2824-1, Vol.2, September, 2004, pp. 190-195.

[2] Mirković, D., Petković, P., "*Multi channel Sigma-Delta A/D converter for integrated power meter*", Proceedings of the Small Systems Simulation Symposium 2010, Niš, Feb., 2010, pp. 90-93.

[3] Stevanović, D., Jovanović, B., Petković, P., Litovski, V., "*Korišćenje snage distorzije za identifikaciju izvora harmonijskog zagađenja na mreži*", Tehnika - Elektrotehnika, 6/2011, Savez inženjera i tehničara Srbije

[4] Stevanović D., "*Metod za efikasnu identifikaciju harmonijskih izobličenja u elektroenergetskoj mreži primenom modifikovanih elektronskih brojila*", Elektronski fakultet u Nišu, 28.12.2015

[5] Dimitrijević, M., "*Elektronski sistem za analizu polifaznih opterećenja baziran na FPGA*", Doktorska disertacija, Niš, 07.12., 2012,