LMS7002M FPRF 2x2 MIMO Transceiver IC With High Digital Content

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Abstract – This paper describes 2TX-2RX MIMO RF IC designed to support a variety of communication standards such as 2G, 3G, 4G and upcoming 5G applications. The chip itself is not particularly designed for those standards so it can be used in wide range of other applications. The chip has been manufactured in sub-micron CMOS technology, packaged in 261 pin aQFN 11.5x11.5 mm package. It is low power design hence typical power consumption is only 880mW in full 2x2 MIMO mode while the chip consumes 550mW in SISO mode.

Keywords – Field programmable RF, transceiver IC, MIMO, wireless communications.

I. Introduction

LMS7002M is a fully integrated, multi-band, multi-standard RF transceiver IC [1] that is highly programmable. It combines Low Noise Amplifiers (RXLNA), TX Power Amplifier Drivers (TXPAD), receiver/transmitter (RX/TX) mixers, RX/TX filters, synthesizers, RX gain control, TX power control, the analog-to-digital and digital-to-analog converters (ADC/DACs) [2][3] and has been designed to require very few external components.

The IC key features are summarized below.

- Field Programmable Radio Frequency (FPRF) chip.
- Dual transceiver ideal for MIMO.
- Continuous coverage of the 100 kHz - 3.8 GHz RF frequency range.
- Programmable RF modulation bandwidth up to 160 MHz using analog interface and up to 60MHz using digital interface.
- Supports both TDD and full duplex FDD.
- Transceiver Signal Processor block employs advanced digital techniques for enhanced performance.
- Low voltage operation, 1.25, 1.4 and 1.8V. Integrated LDOs to run on a single 1.8V supply voltage.
- On chip integrated microcontroller for simplified calibration, tuning and control.
- Integrated clock PLL for flexible clock generation and distribution.
- User definable analog and digital filters for customised filtering.

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Typical applications that LMS7002M has been used so far are:

- Broad band wireless communications.
- GSM, CDMA2000, TD-SCDMA, WCDMA/ HSPA, LTE.
- IEEE® xxx.xxx radios.
- WiFi operating in the Whitespace frequencies.
- Software Defined Radio (SDR).
- Cognitive Radio.
- Unmanned Aerial Vehicle (UAV).

Sections II, III and IV describe circuit functionality while section V presents the most interesting measured performances of the chip

II. Analog and RF Blocks

The top level architecture of LMS7002M transceiver is shown in Figure 1. The chip contains two transmit and two receive chains for achieving a Multiple In Multiple Out (MIMO) platform. Both transmitters share one PLL and both receivers share another. Transmit and receive chains are all implemented as zero Intermediate Frequency (zero IF or ZIF) architectures providing up to 160MHz RF modulation bandwidths (equivalent to 80MHz baseband IQ bandwidth). For the purpose of simplifying this document, the explanation for the functionality and performance of the chip is based on one transmit and one receive circuitry, given that the other two work in exact the same manner.

On the transmit side, In-phase and Quadrature IQ DAC data samples, from the base band processor, are provided to the LMS7002M via the LimeLight™ digital IQ interface. LimeLight™ implements the JESD207 standard IQ interface protocol as well as de facto IQ multiplexed standard. JESD207 is Double Data Rate (DDR) by definition. In IQ multiplexed mode LimeLight™ also supports Single Data Rate (SDR). The IQ samples are then pre-processed by the digital Transceiver Signal Processor (TSP) for minimum analog/RF distortion and applied to the on chip transmit DACs. The DACs generate analog IQ signals which are provided for further processing to the analog/RF section. Transmit low pass filters (TXLPF) remove the images generated by zero hold effect of the DACs, as well as the DAC out-of-band noise. The analog IQ signals are then mixed with the transmit PLL (TXPLL) output to produce a modulated RF signal. This RF signal is then amplified by one of two separate / selectable power amplifier drivers and two open-drain differential outputs are provided as RF output for each MIMO path.

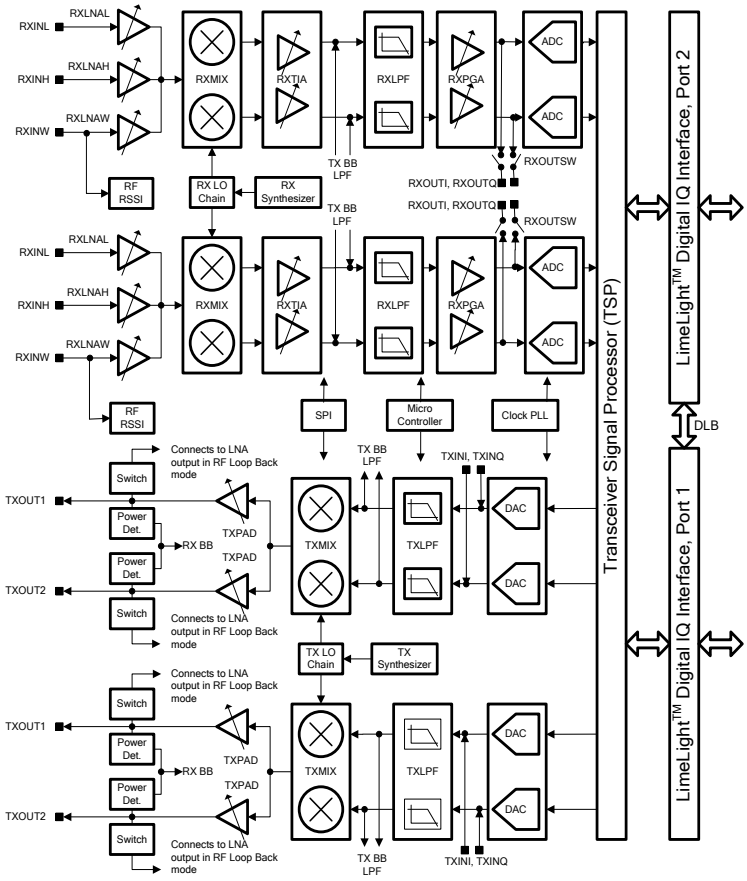

Figure 1: Functional block diagram

The LMS7002M provides an RF loop back option which enables the TX RF signal to be fed back into the baseband for calibration and test purposes. The RF loop back signal is amplified by the loopback amplifier in order to increase the dynamic range of the loop.

There are two additional loop back options implemented, one is an analog base band (BB) loop back and another is a digital loop back (DLB) as shown in Figure 1. The analog loop back is intended for testing while the DLB can be used to verify the LMS7002M connectivity to base band, FPGA, DSP or any other digital circuitry.

On the receive side, three separate inputs are provided each with a dedicated LNA optimised for narrow or wide band operation. Each port RF signal is first amplified by a programmable low noise amplifier (RXLNA). The RF signal is then mixed with the receive PLL (RXPLL) output to directly down convert to baseband. AGC steps can be implemented by a BB trans-impedance amplifier (RXTIA) prior to the programmable bandwidth low pass channel select / anti alias filters (RXLPF). The received IQ signal is further amplified by a programmable gain amplifier RXPGA. DC offset is applied at the input of RXTIA to prevent saturation and to preserve the receive ADC's dynamic range. The resulting analog receive IQ signals are converted into the digital domain with on-chip receive ADCs. Following the ADCs, the signal conditioning is performed by the digital Transceiver Signal Processor (TSP) and the resulting signals are then provided to the BB via the LimeLight™ digital IQ interface.

The analog receive signals can also be provided off chip at RXOUTI and RXOUTQ pins by closing the RXOUT switch. In this case it is possible to power down the on chip ADCs/TSP and use external parts which can be very useful for more resource demanding applications or where higher signal resolution is required. A similar option is also available on the TX side where the analog signal can be processed by external components. The on chip DACs/TSP can be powered down and analog inputs can be provided at TXINI and TXINQ pins.

Two transmitter outputs (TXOUT1, TXOUT2) and three receiver inputs (RXINL, RXINH, RXINW) are provided to facilitate multi-band multi-standard operation.

The functionality of the LMS7002M is fully controlled by a set of internal registers which can be accessed through a serial port and rapidly reprogrammed on the fly for advanced system architectures.

In order to enable full duplex operation, LMS7002M contains two separate synthesisers (TXPLL, RXPLL) both usually driven from the same reference clock source PLLCLK.

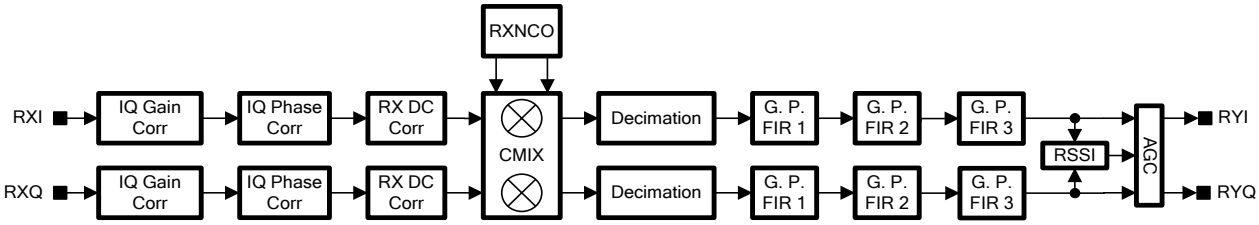

Figure 2: Structure of the RXTSP

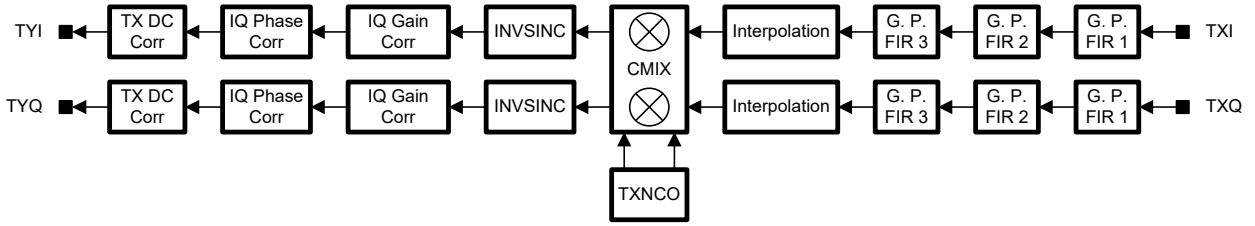

Figure 3: Structure of the TXTSP

III. Digital Transceiver Signal Processing Blocks

LMS7002M includes a high digital gate count within the Transceiver Signal Processor (TSP) block. The function of the TSP is to employ advanced digital signal processing techniques to enhance the performance of the analog/RF parts. This results in an improved performance of the overall system and a saving on total current consumption.

The TSP is placed between the data converters and the LimeLight™ digital IQ interface. Functionally, the RX and TX parts of the TSP are similar, as shown in Figure 2 and Figure 3, respectively.

In both the TX and RX TSP blocks there are three general purpose finite impulse response (FIR) filters, G.P. FIR 1, G.P. FIR 2 and G.P. FIR 3. The filter coefficients are fully programmable and the implementation does not force their impulse response to be symmetrical.

On the TX side, one of these filters could be used as a phase equalizer, which is a requirement in some communication standards such as CDMA2000. Another can be used to flatten the amplitude response of the TXLPF while the third FIR could be used to further enhance the channel filtering function of the BB modem. If phase equalization is not required then one filter can be used to minimize group delay variation of the analog TXLPF.

Possible applications of the G.P. FIR filters on the RX side are similar. One could be used to minimize group delay variation of the analog RXLPF while another could help to improve RXLPF adjacent channel rejection performance.

The interpolation block within the TXTSP takes IQ data from the BB modem and increases the data sample rate. The advantages of having interpolation are as follows. For narrow band systems (GSM/EDGE) or even moderately broad band (WCDMA, CDMA2000) modulation standards, the BB modem does not need to interpolate IQ data to the target system clock. The base band can provide output data at a much lower sample rate saving on power at the digital interface. Having a low data rate interface also simplifies the PCB design. However, the interpolator block generates data samples at the system clock rate, so the DACs run at a high sampling rate. As the DACs are running at a high frequency, it means that the quantization noise is spread over a wider frequency range which results in a better overall SNR. Also, the image generated by the DAC zero hold effect is further away from the wanted signal hence the specification for the TXLPF can be relaxed.

The reason for having decimation in the RXTSP is similar to that of interpolation in TXTSP. The ADCs can run at high frequency, and the specification of the RXLPF used as an anti-alias filter in this case is relaxed, the G.P. FIR improves adjacent channel rejection and the decimation circuit reduces the received data sample rate before sending the data to the BB modem.

The two Numerically Controlled Oscillators (NCO) and digital complex mixer (CMIX) in the TXTSP and RXTSP paths enable the LMS7002M to run in low digital IF.

Inverse sinc filters (INVSINC) within the TXTSP chain compensate for sinx/x amplitude roll off imposed by the DACs themselves.

The Tx DC Corr block is used to cancel residual DC offset of TXLPF. It is also used to cancel TX LO leakage feed-through as mentioned earlier.

There are three sources of the DC component at the RX output. These are the residual DC offset of the RXPGA and RXLPF, RX LO leakage feed-through and second order distortion (IP2). The Rx DC Corr blocks compensate for all of these sources of offset. The block is implemented as a real time tracking loop so any change of the RX DC due to either the signal level change, or due to RX gain change as well as any temperature effect will be tracked and cancelled automatically.

The IQ Gain Corr and IQ Phase Corr blocks correct IQ imbalance in both TXTSP and RXTSP in order to minimize the level of unwanted side band (image) component.

The last stage in the RXTSP path is a digital implementation of an Adaptive Gain Control (AGC) loop. Assuming that the BB modem does not require 12-bit full scale ADC outputs, the digital AGC block can provide a certain level of automatic gain control before the BB involves RF and IF gain stages.

IV. Digital Interfaces and Control

A. LimeLight™ Digital IQ Interface

The LMS7002M implements LimeLight™ digital IQ interface to the BB modem. LimeLight™ can be configured to run in one of the following three modes:

- JESD207 mode
- TRXIQ double data rate (DDR) mode
- TRXIQ single data rate (SDR) mode

All three modes are capable of supporting both TDD and FDD operation. The data throughput of JESD207 and TRX DDR is high enough to connect to up to 2x2 MIMO BB modems.

B. Serial Port Interface

The functionality of the LMS7002M transceiver is fully controlled by a set of internal registers which can be accessed through a serial port interface. Both write and read SPI operations are supported. The serial port can be configured to run in 3 or 4 wire mode with the following pins used:

- SEN serial port enable.
- SCLK serial clock.
- SDIO serial data in/out in 3 wire mode, serial data input in 4 wire mode.
- SDO serial data out in 4 wire mode, don't care in 3 wire mode.

C. On Chip Microcontroller

The LMS7002M can be fully controlled by external BB/DSP/FPGA ICs using 4-wire or 3-wire serial port interface. The controlling processor needs to implement a set of calibration, tuning and control functions to get the best performance out of the transceiver. The on chip microcontroller unit (MCU) provides the option for additional control. This allows the LMS7002M to be independent of the BB/DSP/FPGA and off-loads these devices.

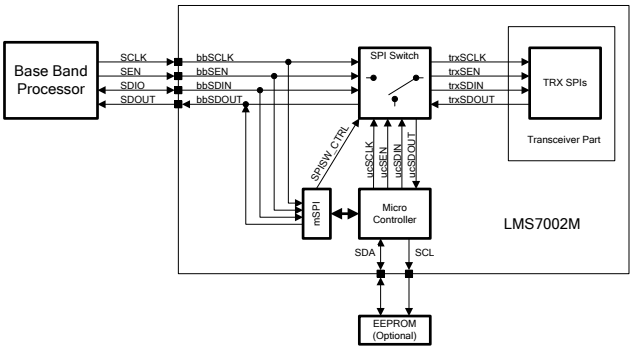

Figure 4: On chip microcontroller connection

MCU integration within the LMS7002M chip is shown in Figure 4. Since the chip communication to the outside world is done through SPI, the MCU uses the same protocol hence the block mSPI (master SPI) is placed in front of it. The MCU communicates to the transceiver circuitry using the same SPI protocol as the BB processor itself. This is implemented via ucSPI lines shown in Figure 4. There is two way communication between the MCU and BB via mSPI. The baseband can trigger different calibration/tuning/control functions the MCU is programmed to perform. The MCU reports a success, failure or an error code back to the base band processor.

In this architecture, the base band processor acts as master since it controls the whole chip, (transceiver as well as MCU). The base band processor also controls the SPI switch (via SPISW_CTRL control bit/line of mSPI) i.e. taking control over the transceiver part or handing it over to the MCU. The MCU acts as a slave processor. It can control the transceiver only if the base band allows that via the SPI switch.

MCU key specifications are as follows:

- 8-bit microcontroller.
- Industry standard 8051 instruction set compatible.
- Memory
  8 KB SRAM program memory
  2 KB SRAM working memory
  256 B dual port RAM
  All on chip, integrated.

D. Data Converters Clock Generation

The clock generation circuit for the data converters is shown in Figure 5. It shares the same reference clock input REFCLK with the RF synthesizers. The clock PLL then generates a continuous frequency range centred around 2.5 GHz. The feed forward divider (FFDIV) is programmable and capable of implementing division values $N = 2(n+1)$, $n = 0, 1, \ldots, 255$

There is a fixed divide by 4 within the ADC block hence clock division on the DAC side to provide more flexibility. There is a MUX to connect either Fpll, or Fpll/M to either ADC or DAC clocks. M is programmable and can be set to $M = 1, 2, 4$ or 8. The other CLKMUX

output will be connected to the other data converter clock input.

TSP blocks receive the same clock as the corresponding data converter, hence there is no need for complex non-power of two or fractional interpolation/decimation. TSP blocks have programmable interpolation/decimation and generate MCLK clocks going back to the base band processor via the LimeLight™ port.

The circuit implements a continuous clock frequency range from 5 MHz to 640 MHz for the data converters.

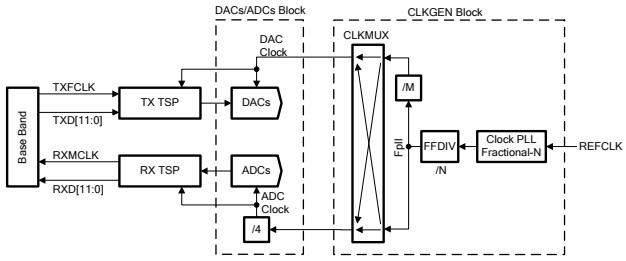

Figure 5: Clock generation and distribution

E. Calibration and Initialization

There are a number of calibrations which the LMS7002M can carry out internally when instructed via the SPI. These calibrations can be initiated on power up/reset to produce optimum settings. Initialization and calibration steps are summarized below.

Initialization

- Power up the chip. In case of using multiple off chip LDOs, power up sequence is not important.
- Apply RESET pulse (active low). This sets all the configuration registers to their default values.
- Overwrite some registers defaults if required.

Available calibration options and recommended order of execution

- TX, RX and clock synthesizer VCO tuning.
- TX and RX analog LPF pass band tuning.
- RX DC offset and RX LO leakage cancellation.
- TX DC offset and TX LO leakage cancellation.
- TX IQ imbalance calibration.
- RX IQ imbalance calibration.

V. Measured Results

Pass band of both transmit and receive analog filters is fully programmable and is tunable up to 80 MHz. Figure 6 illustrates selectivity and tunability of LMS7002M analog filters. This figure shows only low band section of RX filter as an example. Other filters response is similar with the difference that high band sections extend tunability up to 80MHz.

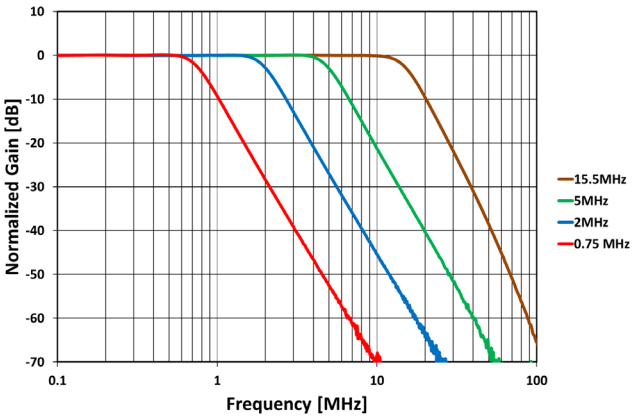

Figure 6: Analog RX LPF amplitude response

LMS7002M transmit output power versus frequency is plotted in Figure 7. Both TX outputs (TX1 and TX2) are measured with obviously different matching networks.

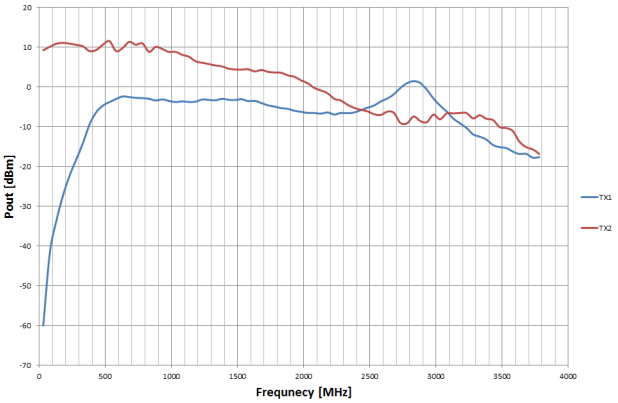

Figure 7: Transmitter gain versus frequency

LMS7002M receiver gain versus frequency is shown in Figure 8. All LNA inputs (LNAH, LNAL, LNAW) are measured. As in the case of the TX chain, different matching networks are used for three RF receiver inputs.

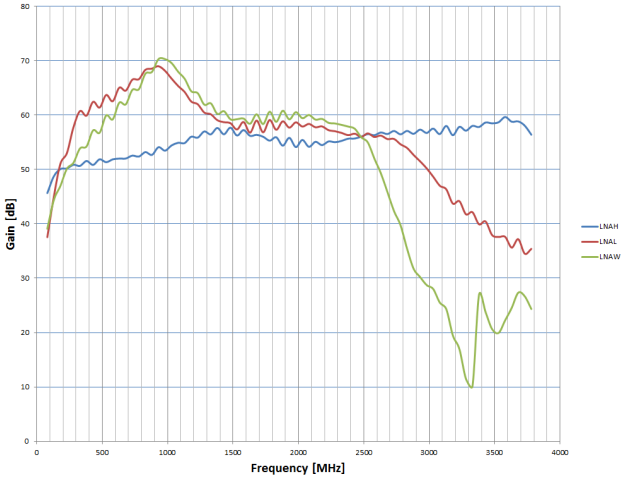

Figure 8: Receiver gain versus frequency

Continuous wave (CW) is used as test signal while measuring TX and RX gain. Figure 7 and Figure 8 show that with proper matching and selecting suitable RX RF input/LNA, LMS7002M provides excellent wide frequency range of operation.

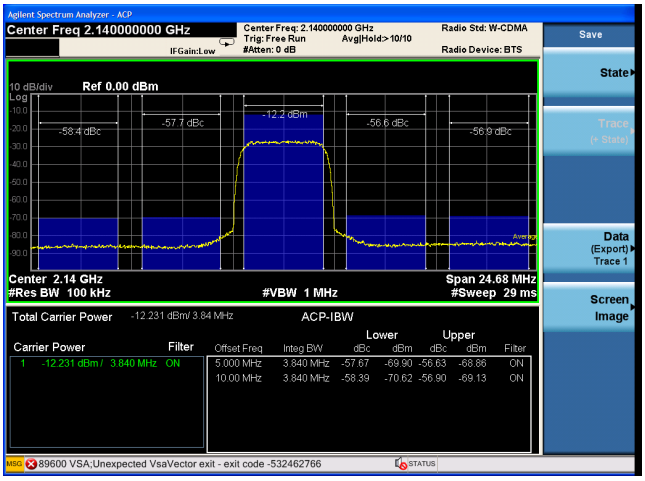

Figure 9: ACPR at 2.14GHz

Adjacent Channel Power Ration (ACPR) is measured using single carrier WCDMA modulated test signal where RF LO is the middle of Band I up link (2.14GHz). Result is shown in Figure 9. Measured ACPR is -56dBc which well over perform the number required by 3GPP standard itself (around -45dBc).

Error Vector Magnitude (EVM) is measured using very demanding 20MHz wide LTE modulated signal. As Figure 10 shows, measured EVM is 1.25% which again outperforms EVM requirement of 3GPP standard (around 8%).

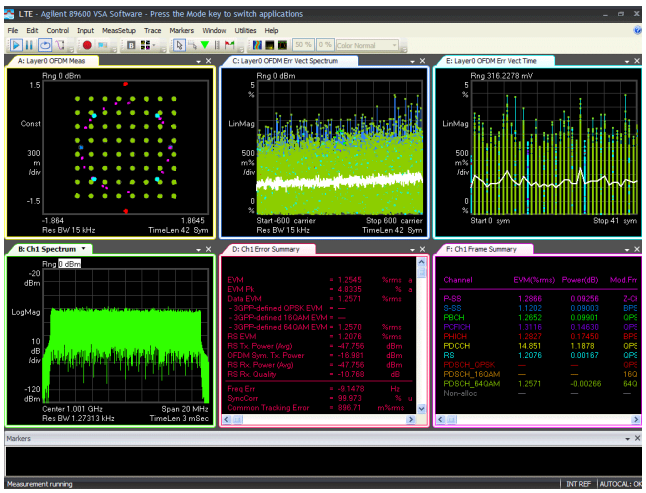

Figure 10: EVM at 1GHz

VI. Conclusion

Very flexible low power MIMO RF IC (LMS7002M) is described in this paper. Measured results show wide frequency range operation of the chip. Also the chip outperforms most of the major communication standards in terms of transmit spectrum mask (ACPR) and modulation accuracy (EVM) leaving excellent margin for the external PA to contribute while still keeping the whole system within the specifications.

References

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