Spice Simulations of Aging Effects in Double-Gate FinFETs

Nebojša Janković, Chadwin D. Young, Miloš Marjanović

Abstract - The electrical characteristics of multi-gate field-effect transistors (FinFETs) suffer from temporal degradations due to hot-carrier injection, bias temperature instability and/or ionizing-radiation damage. The aging effects in FinFETs are mainly caused by cumulative contribution of the simultaneous generation of oxide/Si interface traps and positively charged defects within the gate oxide. The accurate capturing of the dynamic contribution of trapped charges by FinFET electrical models of circuit simulators is important for lifetime prediction and verification of long-term performance of advanced CMOS ICs. In this paper, an auxiliary sub-circuit model of the oxide and interface trapped charges will be used in Spice simualtions of the state-of-art double-gate FinFETs. The good agreement between the simualtion results and the measured change of electrical characteristics of fabricated p-type DG FinFETs under the static and dynamic NBTI tests, was obtained validating the proposed ASC model.

Keywords - Double-Gate FinFET, Trapped charge, SPICE model, device aging, circuit simulation.

I. Introduction

An excellent electrical performance of three-dimensional fin-based Field Effect Transistors (FinFETs), which includes high immunity to short channel effects and CMOS compatible processing, are the key reasons for entering this type of devices in the marketplace [1]. Apart from investigating some unique aspects of these devices, the reliability of highly scaled FinFETs for future CMOS ICs has become major concern and has continuously received the attention of research community [2,3].

Like the conventional planar FET devices, the FinFETs also suffer from temporal degradation (i.e. aging) dominated by bias temperature instability effects [4,5,6]. It arises from cumulative contribution of the generation of oxide/Si interface traps with energy density distribution D_{it} and the generation of positively charged defects in the oxide with areal density N_{ox} [6]. As an example, Fig.1 shows the experimental I_{DS}-V_{GS} characteristics of p-channel DG FinFETs extracted during the negative bias temperature instability (NBTI) stress.

The observed negative voltage shifts and sub-threshold slope degradations of I_{DS}-V_{GS} characteristics with stress time are cased by the increase of D_{it} and N_{ox} trapped charges. The appearance of the NBTI effects and device aging process implies that the accurate capturing of the dynamic contribution of D_{it} and N_{ox} by FinFET electrical models of circuit simulators is important for lifetime prediction and verification of long-term performance of advanced CMOS ICs.

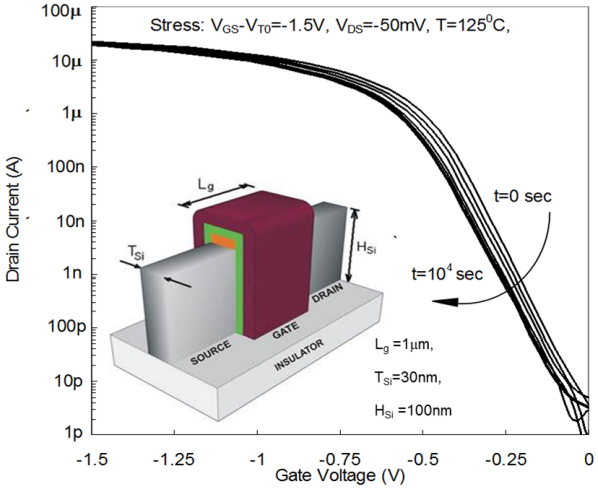

Fig. 1. I_{DS}-V_{GS} characteristics of fabricated p-channel DG FinFETs collected during the NBTI stress. The fabricated device structure is shown in the inset.

So far, the most frequently used multi-gate FinFETs electrical models implemented in Spice (*Simulation Program with Integrated Circuit Emphasis* [7]) were the first industry standard BSIM-CMG model [7,8], the University of Florida double-gate (UFDG) model [9], and the predictive technology model (PTM) [10]. All of these models, however, appear incapable to accurately predict the FinFET temporal degradation and BTI effects, since they neglect the bias-dependence of D_{it} and, moreover, omit N_{ox} as the input parameter. Recently, we have developed an auxiliary sub-circuit (ASC) aimed for proper inclusion of N_{ox} and D_{it} in Spice electrical models of double-gate (DG) FinFETs [11]. In this work, the efficiency of ASC for simulations of the NBTI effects in FinFETs will be demonstrated by comparing Spice modelling results with two dimensional numerical device simulations and the available experiments.

II. The Spice Model of Trapped Charges

In case of fully depleted DG FinFETs with two gates

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shorted (shown in the inset of Fig.1), the implicit equation was derived for calculating the channel potential ψ_s at the front and back surfaces versus the gate-source and the drain-source voltages V_{GS} and V_{DS}, respectively, as [11]:

$$\frac{1}{\gamma^2}\left[\left(V_{GS}-\phi_{ms}+\phi_{nt}-\psi_S\right)^2-\left(V_{GS}-\phi_{ms}+\phi_{nt}-\psi_S+\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}}\right)^2\right]=$$
$$=V_t e^{-(2\cdot\phi_b+b\cdot V_{DS})/V_t}e^{\psi_S/V_t}\left(1-e^{-\frac{q\cdot N_a\cdot t_{Si}^2}{\varepsilon_{Si}\cdot V_t}}\right)+ \quad (1)$$
$$+V_t e^{-\psi_S/V_t}\left(1-e^{\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}\cdot V_t}}\right)+\frac{q\cdot N_a\cdot T_{Si}^2}{\varepsilon_{Si}}$$

where ϕ_{nt} is the flat-band correction potential. Under the assumption of uniform distribution of interface traps over the state energies within the Si bandgap, it can be expressed as [11]:

$$\phi_{nt}=\frac{q}{C_{ox}}\left[N_{ox}-D_{it}\left(\psi_s-\phi_b\right)\right] \quad (2)$$

where also q is the elementary charge, N_a is the fin doping concentration, ε_{Si} is the silicon permittivity, T_{Si} is the fin thickness, $C_{ox}=\varepsilon_{ox}/T_{ox}$ is the gate oxide capacitance per unit area, $V_t=kT/q$ is the thermal voltage, $\phi_b=V_t ln(N_a/n_i)$ is the fin potential, $\gamma=\sqrt{(2\varepsilon_{Si}qN_a)/C_{ox}}$ is the body factor, ϕ_{ms} is the metal-to-semiconductor work function difference.

In order to obtain ψ_s versus V_{GS}, V_{DS} and N_{ox}, D_{it}, the eq. (1) has to be solved iteratively. However, the iterative method is not convenient for device compact modeling. Instead, we have recently developed an auxiliary sub-circuit (ASC) [11] that solves the eq. (1) over ψ_s using Spice simulations. Then, the new Spice model of DG FinFETs including the trapped charges is proposed [11] which combines the industry-standard Spice model BSIM-CMG [13] of multigate FinFETs and the ASC as shown in Fig.2. The ASC effectively function as an ideal voltage controlled voltage source (VCVS) producing the gate correction voltage $\Delta V_{GF}=\phi_{nt}=f(\psi_s)$ between the external and the internal gate nodes G and G*, respectively. Note that ΔV_{GF} diminishes in case of negligible trapped charges (e.g $\Delta V_{GF}\rightarrow 0$ V if N_{ox}, $D_{it}\rightarrow 0$). The ASC schematics and the derivation of model equations were discussed in details in our previous work [11].

III. Simulation Results and Discussion

In Spice simulations, the ASC block serves to correct the input voltage at the gate node of the BSIM-CMG model by the amount of $\Delta V_{GF}=\phi_{nt}$ depending on the assumed values of N_{ox} and D_{it} parameters. Fig.3 shows the comparison between measured and simulated I_{DS}-V_{GS} transfer characteristics collected at t=0 s (fresh device), 215 s and 10^4 s (the end) of the NBTI stress applied at T=125°C with V_{GS}-V_{T0}=-1.5 V, V_{ds}=-50 mV. Good matching between the model and the experiment can be observed in Fig.3 which was accomplished by tuning only the N_{ox} and D_{it} parameters of ASC. Note that a conventional NBTI "stress and sense" approach was employed as a testing method where the stress is interrupted to execute sense I_{DS}-V_{GS} measurements. The experimental p-type DG FinFET devices were fabricated on the (100) SOI substrates and with the gate wrapped around the SOI fin as shown in the inset of Fig.1. Typical device was comprised of 20 fins in parallel with gate length of 1 µm. More details of the DG FinFET design and technology can be found in [14] and [15].

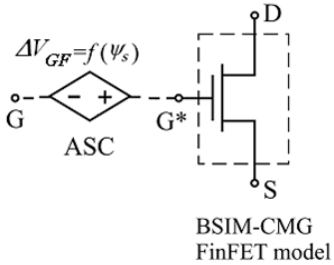

Fig. 2. Spice model of DG FinFET including the NBTI effects.

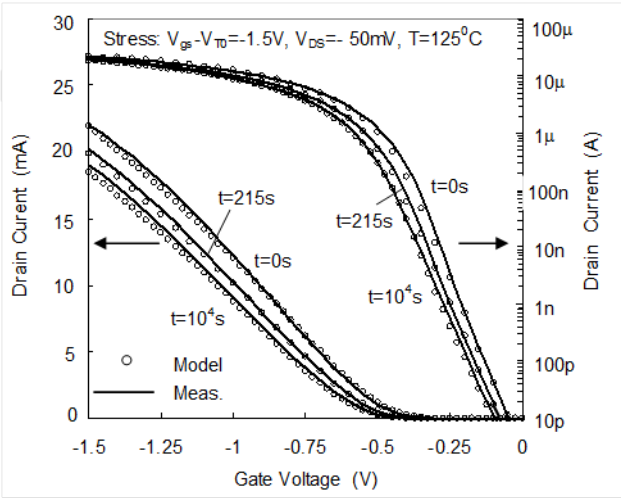

Fig. 3. Examples of measured and simulated I_{DS}-V_{GS} transfer characteristics.

Fig.4 shows the threshold voltage degradation ΔV_T versus the stress time obtained from measured and simulated transfer characteristics of fabricated p-type DG FinFET. Here, ΔV_T is defined as $\Delta V_T=V_{T0}-V_{T,\ stress}$, where V_{T0} and $V_{T,\ stress}$ holds for the threshold voltages of virgin and stressed device, respectively. The V_T extraction method was based on the maximum derivative of the g_m/I_{DS} ratio with respect to V_{GS}, e.g. $V_T=V_{GS}$ for which $d(g_m/I_{DS})/dV_{GS}=0$ [16]. This method was shown to be more

physically adequate for the advanced FinFETs with ultrathin dielectrics, double gate operation and thin SOI body, as is the case with our experimental device [16]. The ±5% error bars appearing in Fig.4 correspond to the largest relative deviation obtained between simulated and measured transfer characteristics in sub-threshold region (Fig.3).

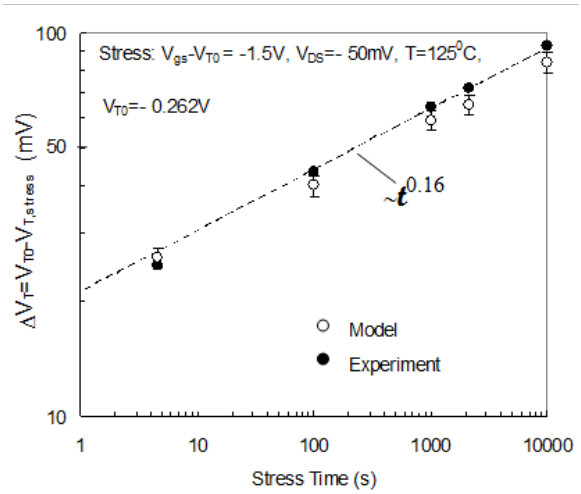

Fig. 4. The dependence of threshold voltage degradation ΔV_T versus the stress time obtained from measured and simulated transfer characteristics.

The aging effects of DG FinFETs subjected to a dynamic NBTI (DNBTI) stress can also be predicted with the ASC model providing that the time and voltage dependent functions $N_{ox}=f(V_{GS}, t)$ and $D_{it}=f(V_{GS}, t)$ are pre-determined and included in (1) and (2). The DNBTI test consists of the high-voltage pulsed periodic signal applied to a gate of FinFET at elevated temperature. During the DNBTI test, the interface defects D_{it} are generated in the on-state time period, while they partially recover in the off-state period of the pulsed signal due to traps annealing [17]. Recently, Kumar et al. [18] have proposed the analytical expressions in the form of $D_{it}= D_{it,\,0}\cdot f(t)$ that hold for time dependence of interface trap density generation in the p-type MOSFETs under the DNBTI stress. We have extended their D_{it} model to include the influence of gate voltage using the semi-empirical expression $D_{it}=A\cdot V_{st}^{m}\cdot f(t)$ where V_{st} is the DNBTI stress voltage while A and the exponent m are fitting constancies. Following the inclusion of D_{it} temporal variations in (1) and (2), we have obtained the drain current degradation $\Delta I_{ON}/I_{ON,0}$ of p-type DG FinFET with L_g=100nm and Tox=1.5nm using Spice simulations with ASC. The DNBTI test was assumed to have the pulsed gate stress signal with 50% duty cycle, 200 s time period and V_{st} of -3.4 V and -2.8 V. The obtained results are shown in Fig.5a. For comparison, Fig.5b shows the experimental results of $\Delta I_{ON}/I_{ON,0}$ obtained for conventional P-type MOSFET with identical geometry as the FinFET and with the same DNBTI test conditions as for Fig.5a. It can be observed that $\Delta I_{ON}/I_{ON,0}$ of both figures are of the same order of magnitude indicating that the aging processe of DG FinFET and planar MOSFETs under the DNBTI tests is quite similar.

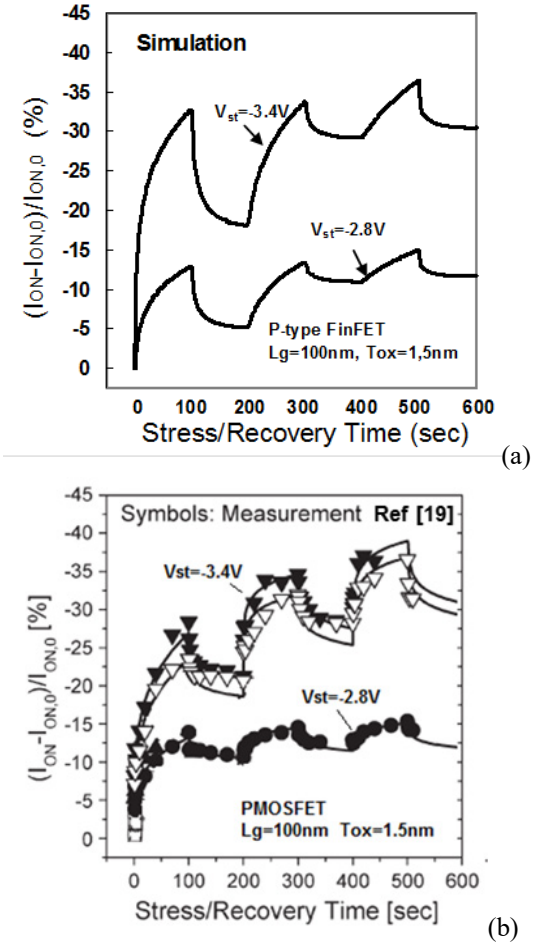

Fig. 5. Simulated (a) and measured (b) drain current degradation $\Delta I_{ON}/I_{ON,0}$ of the p-type FinFET and the planar PMOSFET, respectively, versus the DNBTI stress/recovery time, obtained for various stress amplitude V_{st}, of the 200 s period pulsed signal and with V_{ds}=-50 mV.

IV. Conclusion

A practical impelementation of the auxiliary sub-circuit (ASC) derived for Spice simualtions of NBTI effects in DG FinFETs was described in this work. The good agreement between the simualtion results obtained using the industry-standard BSIM-CMG model with ASC and the measured change of electrical characteristics of fabricated p-type DG FinFETs under the static and dynamic NBTI tests, was obtained validating the proposed ASC model.

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