Self-Heating Assessment for Interconnects During ESD Event

Vazgen Melikyan, Ararat Khachatryan and Davit Mirzoyan

Abstract –During ESD event the metal interconnects can be impacted due to Joule heating. A self-heating model for metal interconnects has been proposed for providing a realistic assessment of current and interconnect performance during ESD event. This model is matching with experimental results, and it can be used to forecast TLP I(V) characteristics of isolated metal wires.

Keywords – Interconnects, self-heating, ESD event, Joule heating.

I. Introduction

During ESD event a high Joule heating is a major cause of failure in metal interconnects and this could be enhanced by using of low-k material as interlayer dielectric, since such materials exhibit poor thermal properties. In fact, the increase in current densities in metallic interconnections, and the subsequent self-heating are particularly destructive [1,4]. ESD discharges can cause both latent and permanent damages in interconnections. In metal based interconnect the self heating effect leads to permanent resistance change and reduces the electromigration lifetime significantly [5,6]. Moreover, as the temperature variation increases the metal lines resistance [8,9], the voltage drop across the ESD protection path is strongly impacted. Thus, it is crucial for supporting ESD designers to develop a scalable compact model able to take self-heating effect into account and included a failure criterion in order to predict the transient and quasi-static behavior of an interconnection as well as its failure [1,6]. In order to provide a realistic assessment of current and future interconnect performance, a self heating model for isolated metal lines, valid in the ESD time range, is developed. This model will be compared experimental results in 45nm and 130nm technology, and it will be used to forecast TLP I(V) characteristics of isolated metal wires

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II. Interconnect Model

A. Model Equations

Since the increase in temperature of a metal line seems to be the main parameter accountable of the failure, in many works authors have sought to simulate the temperature rise due to Joule self-heating in the metal line. In the HBM to CDM time domain the adiabatic assumption cannot be applied and the heat diffusion in the dielectric has to be taken into account. Contrary to [1, 9] which use a thermal RC network with a constant thermal capacitance, [2] assumes that there is a volume of dielectric within a thermal diffusion length (not constant during the transient event) which is at the same temperature as the metal. By solving the heat equation (1), which links the temperature T and the current density j of the considered material, [2] establishes the expression of the total thermal capacitance of an interconnection (2).

$$\rho * c\left(\frac{\partial T}{\partial t}\right) = \nabla(k * \nabla T) + \rho_e(T) * j^2 \qquad (1)$$

Where ρ is material density, ρ_e electrical resistivity, c specific heat and k thermal conductivity.
The total thermal capacitance is the sum of the thermal capacitance of the metal, C_{THM}, and the thermal capacitance of the dielectrics enclosing it, C_{THD}:

$$C_{TH}=C_{THM}+C_{THD} \qquad (2)$$

Where

$$C_{THM}=c_M*V_{METAL} \qquad (3)$$

$$C_{THD}=c_{IMD}*V_{IMD}+ c_{ILD}*V_{ILD} \qquad (4)$$

c_M, c_{IMD} and c_{ILD} are respectively the specific heat coefficients of the metal interconnect, the inter-metal dielectric (IMD) and the inter-layer dielectric (ILD) as illustrated in the figure 1.

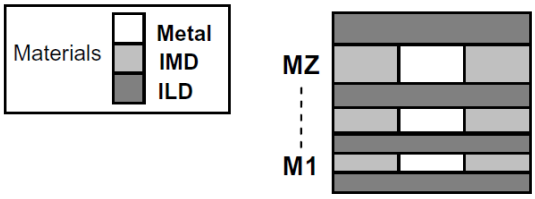

Fig. 1. Cross section of metal layers stacked

The heat conduction volumes of each material, V_{METAL}, V_{IMD} and V_{ILD}, depend on the interconnect geometrical specifications, L, H and W, as shown in figure. As the dielectrics heat conduction volumes are calculated from the interconnects dimensions in order to have a scalable model, two shape factors s_L for the IMD and s_v for the ILD, are introduced.

$$V_{METAL}=L*H*W \quad (5)$$
$$V_{IMD}=2s_L*L*H*W_{DIFF} \quad (6)$$
$$V_{ILD}=2s_VL*W*H_{DIFF} \quad (7)$$

W_{DIFF} and H_{DIFF} are respectively the thermal diffusion lengths of the IMD and the ILD as illustrated in the figure 2.

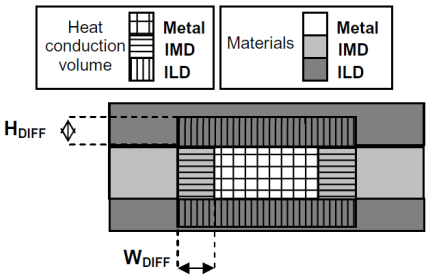

Fig. 2. Cross section of a metal layer during the heat dissipation

Those dimensions are directly linked to the time and the thermal diffusion coefficients of the inter-metal dielectric, α_{IMD}, and the inter-layer dielectric, α_{ILD}, following those equations:

$$W_{DIFF} = \sqrt{\alpha_{IMD} t} \quad (8)$$
$$H_{DIFF} = \sqrt{\alpha_{ILD} t} \quad (9)$$

The temperature variation is directly linked to the electrical energy dissipation, E, and thermal capacitance of the interconnection, C_{TH}:

$$E(t) = C_{TH} * \Delta T(t) \quad (10)$$

The energy needed to increase the system temperature is provided by Joule heating (11).

$$E(t) = \int_0^{\Delta t} R(t) i^2(t) dt \quad (11)$$

Then, the metal resistivity dependence with temperature has been assumed to be linear. Thus, a temperature variation, _T, leads to a variation of the interconnect resistance, R, according to the following equation:

$$R = R_0(1 + TCR \times \Delta T) \quad (12)$$

R_0 is the resistance value at the reference temperature and TCR is the temperature coefficient resistance. [3] asserts that resistance increases linearly with the energy, even through the metal phase change from solid to a liquid, whereas, [1] uses two different TCR values, one corresponding to the solid phase of the metal line and the second to its liquid phase. In this paper there is chosen one TCR coefficient which is sufficient to model accurately the linear resistor variation during the transient event (figure 8). The resistance R0 is defined by the metal resistivity, ρ, and the geometrical specifications of the interconnection: the length, L, the height, H and the width, W, as depicted in the figure 1:

$$R_0 = \rho \frac{L}{H*W} \quad (13)$$

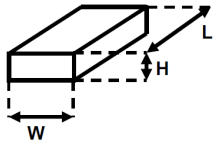

Fig. 3. Geometrical specifications of an interconnection

In order to have a scalable model of self heating the equivalent thermal capacitance is defined by the interconnect dimensions as:

$$C_{TH}(t) = \left(c_M + c_D\delta(t)\right) * L * H * W \quad (14)$$

Where

$$C_D = c_{ILD} + c_{IMD}$$
$$\delta(t) = \sqrt{\alpha_D t} \quad (15)$$

The α_D parameter integrates the thermal diffusion coefficients and the shape factors of heat conduction volumes of the dielectrics.

B. Metal failures under high current short pulses

Metal wires exposed to ESD stresses, and more generally to short-time high current pulses, show thermally accelerated open circuit failures [2]. The temperature rise in interconnect appears to be the main parameter which controls the metal failure. In [3] there is shown that the failure temperature of a passivated metal line should be included between its melting temperature (660 °C) and its evaporation temperature (2467 °C). Experimentally, [2] uses the DC resistance thermometry to assess the temperature rise in passivated metal wire. Based on element simulations and measurements, there is shown that the metal open always occurs at the same temperature rise, which is over 1000 °C. As the copper melting temperature is 1084 °C [1] and according to [6], it is supposed that the critical temperature leading to an open failure is above this value. All these considerations have lead to introduce the metal melting temperature, T_{MAX}, in the model as a failure criterion. If the metal line temperature exceeds this limit the interconnection resistance takes an infinite value. The impact of multiple stresses on the resistance is not taken into account in the model. Nevertheless, a second temperature threshold can be

introduced in order to take into account the reliability reduction by sending a warning message to caution designers that latent damages can appear in interconnections. This temperature threshold can be linked to the current level that causes an electromigation lifetime reduction [5] (around 50% of the failure current). After having defined the failure criterion, the scalability of the αD parameter should be examined.

III. Parameter Extraction

The specific heat coefficients, the resistivity and the height of the interconnection is technological data. The 45nm and 130nm technology nodes information were used as an experimental results. In order to extract the parameter αD, a methodology based on the following steps must be used on transient characterizations as illustrated in figure 4.

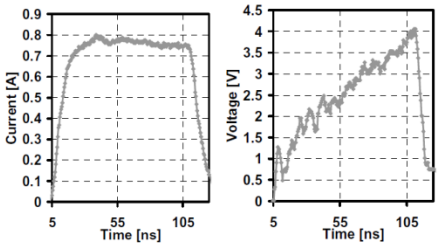

Fig. 4. Voltage and current chronograms of an interconnection for a TLP voltage pulse with a 100ns duration.

First, it's necessary to calculate the energy and the temperature during the transient event as (figure 5):

$$E(t) = \int V(t)I(t)dt \tag{16}$$

$$\Delta T(t) = \frac{1}{TCR}\left(\frac{\frac{V(t)}{I(t)} - R_0}{R_0}\right) \tag{17}$$

Knowing, the specific heat coefficient and the interconnects dimensions, the function δ(t),depicted in figure 6, can be calculated as :

$$\delta(t) = \frac{1}{c_D}\left(\frac{1}{L*H*W}\frac{E(t)}{\Delta T(t)} - C_M\right) \tag{18}$$

Finally, αD can be extracted easily from the δ(t) curve.

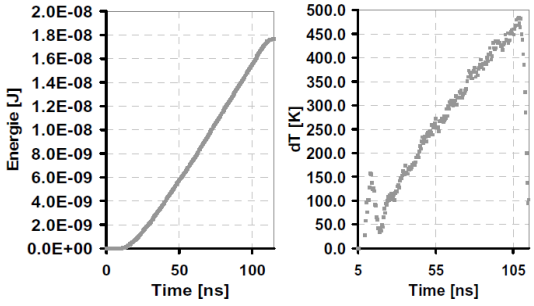

Fig. 5. Energy and temperature chronograms of an Interconnection (TLP voltage pulse, 100ns duration)

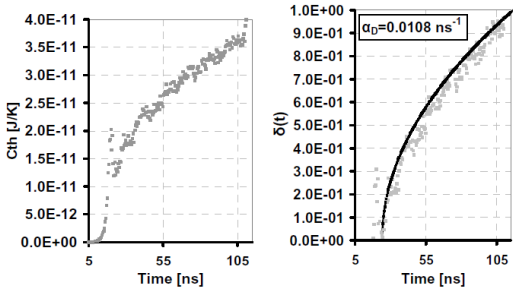

Fig. 6. Equivalent thermal capacitance and function δ(t) of an interconnection (TLP voltage pulse, 100ns duration)

The extraction results presented in figure 7 show that αD only depends of the metal layer and also of the interconnect height. The value of αD is sensibly equal for M1 and MX metal layer. This is due to the metal thickness which is the approximately the same for those metal layers as the dielectrics around the interconnections. As the thickness of the metal layer MZ is higher than the M1 layer thickness the dielectrics volume used for the heat dissipation is smaller than the metal volume which is bigger due to its thickness. As the dielectrics contribution concerning the heat dissipation is smaller the αD value of the MZ layer is clearly lower. The width seems to have few impacts on the αD parameter.

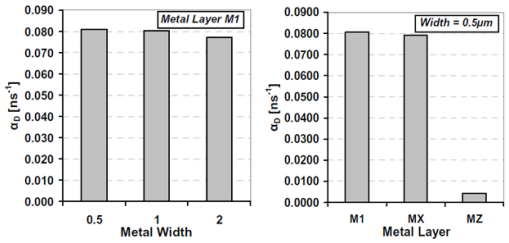

Fig. 7. α_D coefficient value for different widths of metal layers

IV. Validation

As depicted in figure 8, the simulated voltage of an interconnection fits perfectly the measurement data for a TLP voltage pulse with 100ns duration. It can be concluded that the self-heating effect is correctly reproduced during the transient event.

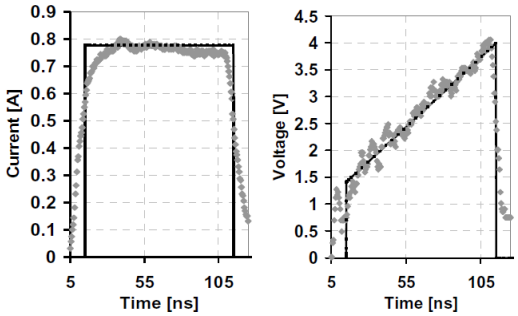

Fig. 8. Voltage and current chronograms of an Interconnections (TLP voltage pulse, 100ns duration) Measurement – Gray, simulation – Black

Then, simulations corresponding to TLP and VF-TLP characterizations using a 50_ impedance were performed for different pulse duration (100ns, 30ns, 10ns) as illustrated in the figures 9, 10 and 11. The averaging window applied on simulated chronograms and measurements for each TLP pulse is defined between 60% and 80% of the pulse duration. By applying this averaging of each simulated pulse we have built the TLP IV curves. The simulated results provided by the compact model are well correlated with measurements.

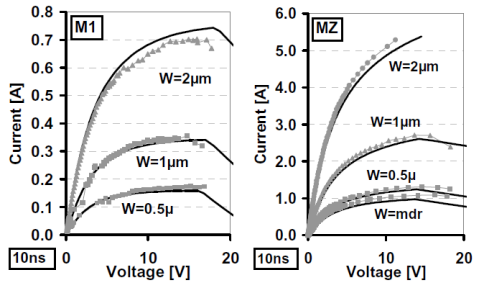

Fig. 9. VF-TLP IV curves of interconnections, 45nmtechnology: two metal layers M1 and MZ, measurements Gray and simulations Black for 10ns square pulses

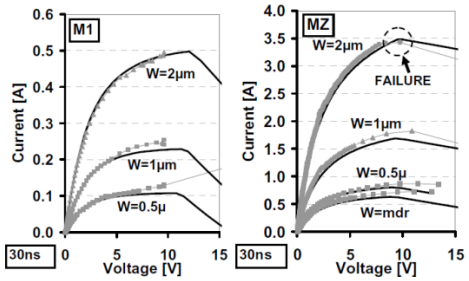

Fig. 10. VF-TLP IV curves of interconnections, 45nm technology: two metal layers M1 and MZ, measurements-Gray and simulations Black for 30 ns square pulses

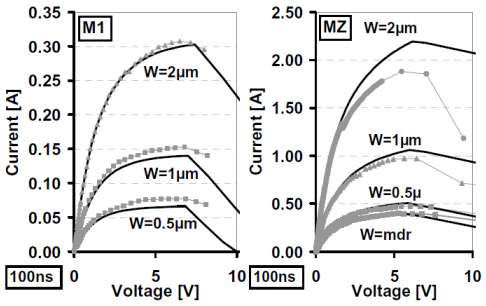

Fig. 11. VF-TLP IV curves of interconnections, 45nm technology: two metal layers M1 and MZ, measurements - Gray and simulations - Black for 100 ns square pulses.

Then, when the interconnection reaches the metal melting temperature the model resistor has a high value in order to reproduce an open circuit failure as explained in II.B. Thus, it is observed a kink in simulated curves. As the metal melting temperature provides a good estimation of the interconnects failure, it can be considered as a valuable failure criterion.

VI. Conclusion

High Joule heating during ESD event is a major cause of failure in metal interconnects. To provide a realistic assessment of current and future interconnect performance, a compact model of self heating in isolated metal lines, valid in the ESD time range (time <100ns), has been proposed. The results with this model matching with experimental results performed in 45nm and 130nm technology, and it can be used to forecast TLP I(V) characteristics of isolated metal wires.
Moreover this model only required the extraction of a single model parameter for each metal layer. Without a complete thermal RC network on contrary with [1, 9], but using only a thermal capacitance the model provides a matching with measurements maximum by 9% tolerance and a prediction concerning the failure by 5% tolerance.

References

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